

JUN 20 2008

**FAX COVER SHEET**

The information contained in this facsimile message, if a client of this firm is a named addressee, or the message is otherwise intended for a client, is presumptively legally privileged and confidential information. If you are not a named addressee, or if there is any reason to believe that you may have received this message in error, (1) do not read the message below; (2) do not distribute or copy this facsimile; and (3) please immediately call us collect at the number of the sender below.

DATE: June 20, 2008**TOTAL # OF PAGES:**
(INCLUDING THIS COVER SHEET) 3**TO:** Examiner Shambhavi Patel**FAX #:** 571-273-8300**FIRM NAME:** U.S. Patent & Trademark Office**PHONE #:** 571-272-5877**FROM:** Josh Engel**FAX #:** (303) 629-3450**PHONE #:** (303) 352-1139**EMAIL:** engel.josh@dorsey.com**COMMENTS:**

Attached please find the Agenda for the Examiner Interview on June 24, 2008 at 12:00 p.m. MST regarding the below patent application:

Application No. 10/774,990
Filing Date: 02/09/2004
Inventor: Matthew J. Amatangelo
Attorney Docket: 188082/US
Confirmation No. 9588
Art Unit: 2128
Office Action Date: 02/28/08

ORIGINAL WILL NOT BE SENT

PLEASE CONTACT PAULA EGOLF AT 303-352-1175 IF THIS TRANSMISSION IS INCOMPLETE OR CANNOT BE READ.

REFERENCE #481214-24 (188082/US)

DORSEY & WHITNEY LLP · WWW.DORSEY.COM · T 303.629.3400 · F 303.629.3450
REPUBLIC PLAZA BUILDING · SUITE 4700 · 370 SEVENTEENTH STREET · DENVER, COLORADO 80202-5647
USA CANADA EUROPE ASIA

Agenda for Examiner Interview on 6-24-08, 12 pm MST re: application 10/774,990

1. 112 Rejections

a. Indefiniteness rejections

1. Particular terms

- i. evaluate node – see Zhao reference, section I, 2nd paragraph, also see application para. 34
- ii. dynamic circuit – common in the art (see textbook figures)
- iii. labeling – see application para. 42 (labeling = inserting a keyword)
- iv. near dynamic circuit – see application para. 9 (near domino is a species of the genus near-dynamic, just as domino is a species of the genus dynamic)
- v. dynamic signal – common in the art

b. Incomplete rejection (omitting essential steps)

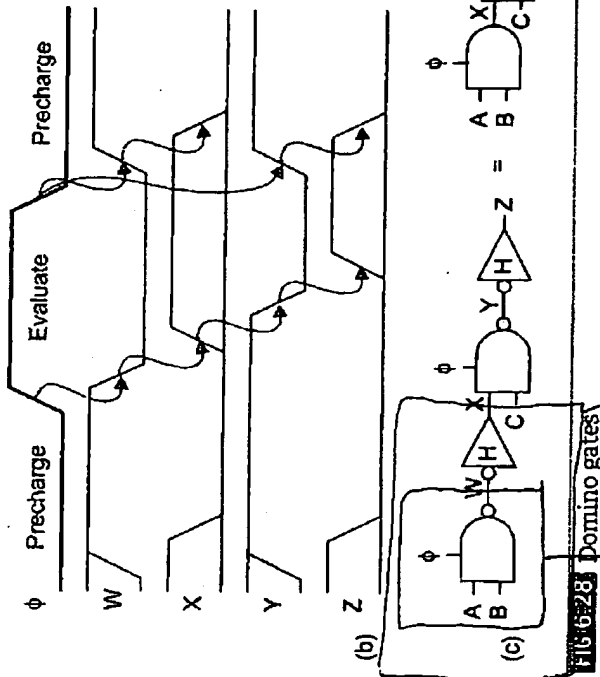
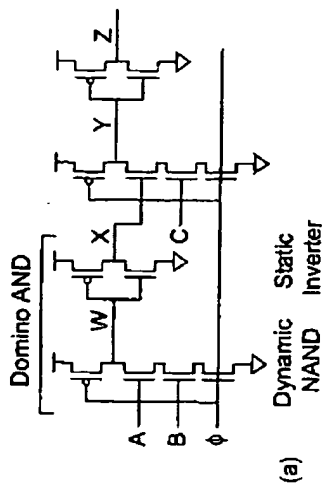
1. ??

2. 101 Rejections

- a. proposed change 'propagating' to 'modeling' in claim 1

3. 102 Rejections

- a. Norton labels the nodes as either clock, data, dynamic, latch, or gated. The present invention labels them as "near dynamic"



true domino
true dynamic

From CMOS VLSI Design
A Circuits and Systems Perspective
(3rd Edition)
Neil Weste and David Harris
Addison Wesley
ISBN: 0-321-14901-7

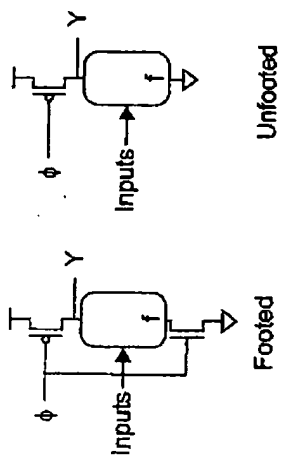


FIG 6-24 Generalized footed and unfooted dynamic gates

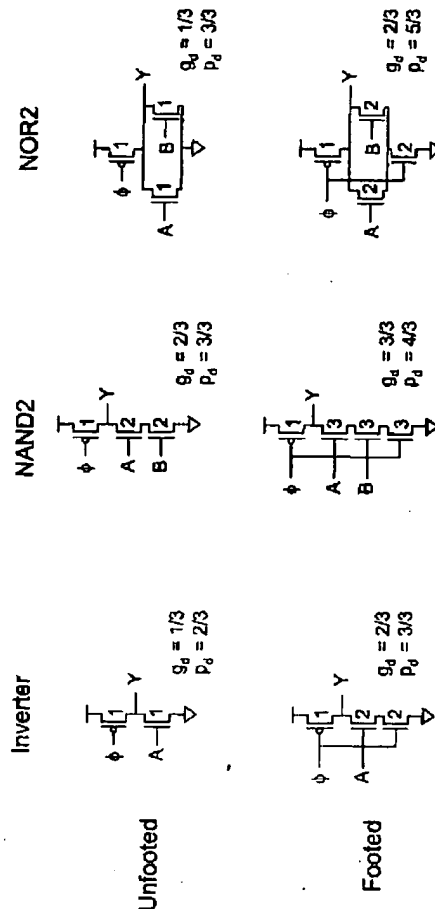


FIG 6-25 Catalog of dynamic gates

Copyright © 2005 Pearson Addison-Wesley. All rights reserved.